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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 08/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/435,448	YAMADA, YASUYOSHI	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19,21 and 23-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21 and 23-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The reply filed on 5-20-4 is not fully responsive to the prior Office Action because it fails to conform to the provisions of MPEP 714.03:

> 37 CFR 1.111. Reply by applicant or patent owner to a non-final Office action.
>
> (b) In order to be entitled to reconsideration or further examination, the applicant or patent owner must reply to the Office action. The reply by the applicant or patent owner must be reduced to a writing which distinctly and specifically points out the supposed errors in the examiner's action and must reply to every ground of objection and rejection in the prior Office action. The reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references. If the reply is with respect to an application, a request may be made that objections or requirements as to form not necessary to further consideration of the claims be held in abeyance until allowable subject matter is indicated. The applicant's or patent owner's reply must appear throughout to be a bona fide attempt to advance the application or the reexamination proceeding to final action. A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references does not comply with the requirements of this section.
>
> (c) In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.
>
> Where a bona fide response to an examiner's action is filed before the expiration of a permissible period, but through an apparent oversight or inadvertence some point necessary to a complete response has been omitted - such as an amendment or argument as to one or two of several claims involved or signature to the amendment - the examiner, as soon as he or she notes the omission, should require the applicant to complete his or her response within a specified time limit (usually one month) if the period for response has already expired or insufficient time is left to take action before the expiration of the period. If this is done the application should not be held abandoned even though the prescribed period has expired.

Specifically, the 37 CFR 1.75(c) objection of claim 8 has not been addressed.

Because the response appears to be bona fide, but through an apparent oversight or inadvertence the response is incomplete, and in order to continue to afford applicant the benefit of compact prosecution, the requirement to complete the response within a one month time limit is

waived, the amendment is entered, and the claims are examined on the merits.

Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. To further clarify, claim 8 refers only to the back electrode electronic part element of claim 7, but claim 7 comprises additional limiting elements not referred to by claim 8.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 19 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 19 this insufficient antecedent basis for the language "said electronic."

In claim 24 this insufficient antecedent basis for the language "the first one of the plurality of integration electrodes."

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4-6, 13-15, 21 and 25-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Barrow (6118182).

At column 1, lines 5-21; and column 2, line 8 to column 4, line 9, Barrow discloses the following:

A back electrode electronic part comprising: a main body 12; a circuit; and electrodes arranged on an outer back surface 16 of the main body; wherein; the electrodes comprise integration possible electrodes 18

and general electrodes 18; a plurality of the said integration possible electrodes are arranged adjacently to each other to form a group of integration possible electrodes; the group of integration possible electrodes is connected to a single first solder bump "robust solder joint" 26; each of the general electrodes are individually connected to single second solder bumps 26; the first solder bump is larger than each of the second solder bumps; and each of the integration possible electrodes that are part of the group of integration possible electrodes inherently have a substantially same potential level when said circuit operates; wherein said electrodes are arranged in a matrix, and said group of integration possible electrodes is arranged at a corner of the matrix; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes inherently comprises a signal electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a ground potential electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power supply potential electrode; wherein said group of integration possible electrodes is directly connected to said first solder bump; wherein said electrodes arranged on an outer surface of the main body of the back electrode electronic part protrude from said back electrode electronic part so as to support said first and second solder

bumps; wherein the outer surface of the main body is a rearmost surface of said back electrode electronic part; wherein four "at least two" integration electrodes form the group of integration possible electrodes; wherein three integration electrodes form the group of integration possible electrodes; wherein a first and second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a ground electrode and an inherently non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a signal electrode and a non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power electrode and a non-contact electrode, respectively.

A back electrode electronic part comprising: a main body including a circuit; and electrodes arranged for solder bumps and supported on an outer back surface portion of said electronic part and connected to said circuit; wherein said electrodes are arranged into groups of electrodes 18 at portions of the electrode arrangement; at least one of said groups of electrodes is connected to a first solder bump 26 which is larger than second solder bumps 26 connected to said electrodes arranged other than in said groups of electrodes; the electrodes arranged other than in said groups of electrodes

are each connected to only one second solder bump; said groups of electrodes having a substantially same potential level when said circuit operates.

To further clarify the disclosure that the first solder bump is larger than each of the second solder bumps, Barrow discloses that the first bump comprises two second bumps; therefore, it is larger than the second bumps. In addition, Barrow discloses that the "pad [electrode] has a width that is less than a length," and that the bumps, "typically reflows into the rectangular shape of the contact pad"; hence, Barrow discloses that the first bump has a width that is less than a length. Similarly, Barrow disclose that the first bump has "a relatively long length," and, "additional length." Therefore, the first bump has a larger lengthwise lateral cross section than the widthwise lateral cross section of the second bump. Indeed, the totality of the disclosure, including the drawings, discloses that the first solder bump is larger than each of the second solder bumps.

Also, although Barrow explicitly discloses wherein one of said electrodes of said group is a ground potential electrode, and wherein one of said electrodes of said group is a power supply potential electrode, the intended uses of the electrodes as ground and power electrodes do not result in a structural difference between the claimed electrodes and the electrodes of Barrow. Further, because the electrodes of Barrow are

inherently capable of being used for the intended uses, the statements of intended use do not patentably distinguish the claimed electrodes from the electrodes of Barrow.

Similarly, although Barrow does not appear to explicitly disclose wherein one of said integrated electrodes of said group is a signal electrode, this intended use of the electrode does not result in a structural difference between the claimed electrode and the electrode of Barrow. Further, because the electrode of Barrow is inherently capable of being used for the intended use, the statement of intended use does not patentably distinguish the claimed electrode from the electrode of Barrow.

Further, although Barrow does not appear to explicitly disclose that each of the integration possible electrodes that are part of the group of integration possible electrodes inherently have a substantially same potential level when said circuit operates, this limitation is an inherent property of the integration possible electrodes of Barrow because they are electrically interconnected by the first bump. In any case, the limitation, "when said circuit operates," is a statement of intended use which does not result in a structural difference between the claimed electrodes and the electrodes of Barrow. Further, because the electrodes of Barrow are inherently capable of being used as intended, the statement of intended use does not patentably distinguish the claimed electrodes from the electrodes of Barrow.

To further clarify the disclosure of an inherently non-contact electrode, it is noted that the electrode 18 is not in direct physical contact with another electrode 18; therefore, it is a non-contact electrode with respect to direct physical contact with another electrode.

Claims 3, 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrow as applied to claim 1 supra, and further in combination with Kaneshiro (JP10-56093).

Barrow does not appear to explicitly disclose wherein one of the integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode which is not connected to said circuit, and wherein a second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode.

Nevertheless, in the figures, and English translation and abstract, Kaneshiro discloses one of integration possible electrodes 10 of a group is a non-contact electrode (associated with "non contact electrode (N)") which is not connected to a circuit. Moreover, it would have been obvious to provide the electrode of Barrow with the non-contact property of Kaneshiro because, as taught by Kaneshiro, it would improve connection strength and reliability and facilitate production of a BGA device ("double with the specification of a BGA type semiconductor device").

Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrow (6118182).

Barrow is applied for the same reasons it was applied to claim 1, supra.

However, Barrow does not appear to explicitly disclose wherein each of the electrodes are the same size; wherein a first distance between a first and second one of the plurality of integration electrodes forming the group of integration possible electrodes is the same as a second distance between the first one of the plurality of integration electrodes and a nearest one of the general electrodes.

Nonetheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied prior art, the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using other dimensions. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531

F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 7-12, 16-19 and 27-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barrow as applied to claims 1, 2, 4-6, 13-15, 21 and 25-29 supra, and further in combination with Ikegami (JP10303249).

As cited supra, Barrow discloses the following:

An electronic assembly comprising: a back electrode electronic part comprising: a main body; a circuit, and electrodes arranged on an outer back surface of the main body, wherein the electrodes comprise integration possible electrodes and general electrodes; a plurality of the integration possible electrodes are arranged adjacently to each other to form a group of integration possible electrodes; each of the integration possible electrodes that are part of the group of integration possible electrodes have a substantially same potential level when said circuit operates; said electronic assembly further comprising: a printed circuit board 28; said group of integration possible electrodes and said circuit board are connected to a single first solder bump; each of said general electrodes and said circuit board are individually connected to single second solder bumps; and said first solder bump is larger than each of the second solder bumps; wherein said electrodes of said back electrode electronic part are arranged in a

matrix, and said group of integration possible electrodes is arranged at a corner of the matrix; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode which is not connected to said circuit; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes inherently comprises a signal electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a ground potential electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power supply potential electrode; wherein said group of integration possible electrodes is directly connected to said first solder bump; wherein said electrodes arranged on an outer surface of the main body of the back electrode electronic part protrude from said back electrode electronic part so as to support said first and second solder bumps; wherein the outer surface of the main body is a rearmost surface of said back electrode electronic part.

A back electrode electronic part comprising: at least two first electrodes 18 positioned on an outer rear surface of said electronic part and connected to a first solder bump 26; at least one second electrode 18 positioned on the outer rear surface of said electronic and connected to a second solder bump 26 wherein said first solder bump has a larger lateral

cross section than said second solder bump; and each of said first electrodes and second electrode are arranged in a matrix on said rear surface of said electronic part so that the first electrodes are spaced apart; wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a ground electrode and a non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a signal electrode and a non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a power electrode and a non-contact electrode, respectively.

However, Barrow does not appear to explicitly disclose wherein each of the electrodes of the back electrode electronic part are the same size; and wherein the first electrodes are spaced apart by the same distance that the second electrode is spaced apart from a nearest one of the first electrodes.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied

prior art, the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using other dimensions.

Also, Barrow does not appear to explicitly disclose substrate electrodes arranged on an outer surface of the printed circuit board, wherein: the substrate electrodes comprise a first substrate electrode and second substrate electrodes; said first substrate electrode is connected to a single first solder bump; each of said general electrodes and each of said second substrate electrodes are individually connected to single second solder bumps; wherein said first substrate electrode of said printed circuit board is larger than each of said second electrodes of said printed circuit board.

Still, in the drawings, and English abstracts and translations, Ikegami discloses substrate electrodes arranged on an outer surface of the printed circuit board 5, wherein: the substrate electrodes comprise a first substrate electrode 18 and second substrate electrodes 6; said first substrate electrode is connected to a single first solder bump 17; each of said second substrate electrodes are individually connected to single second solder bumps 3; wherein said first substrate electrode of said printed circuit board is larger than each of said second electrodes of said printed circuit board. Moreover, it would have been obvious to combine the electrodes of Ikegami

with the product of Barrow because it would enable connection of the circuit board and bumps of Barrow.

In addition, Barrow does not appear to explicitly disclose wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode which is not connected to said circuit.

Notwithstanding, as cited, Ikegami discloses non-contact "dummy" electrodes 17, 18 which are not connected to a circuit. Furthermore, it would have been obvious to combine the non-contact electrodes of Ikegami with the product of Barrow because it would facilitate bump connection inspection and testing.

Claims 1, 2, 4-8, 10-19, 21 and 23-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dockerty (5796169) and Barrow (6118182).

At column 2, lines 27-44; column 3, lines 1-5, 16-30 and 48-61; column 4, lines 23-26; column 4, line 35 to column 5, line 23; column 5, lines 38-67; and column 6, line 59 to column 7, line 11, Dockerty discloses the following:

A back electrode electronic part comprising: a main body 3; a circuit; and electrodes arranged on an outer back surface of the main body; wherein; the electrodes comprise inherently integration possible electrodes

15 and general electrodes 14; a plurality of the said integration possible electrodes are arranged adjacently to each other to inherently form a group of integration possible electrodes; the integration possible electrodes are connected to a single first solder bump 16/33; each of the general electrodes are individually connected to single second solder bumps 11; the first solder bump is larger than each of the second solder bumps; wherein said electrodes are arranged in a matrix, and said group of integration possible electrodes is is arranged at a corner of the matrix; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a signal electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a ground potential electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power supply potential electrode; wherein said group of integration possible electrodes is directly connected to said first solder bump; wherein said electrodes arranged on an outer surface of the main body of the back electrode electronic part protrude from said back electrode electronic part so as to support said first and second solder bumps; wherein the outer surface of the main body is a rearmost surface of said back electrode electronic part; wherein a first and second one of said integration possible electrodes that are part of said group of integration

possible electrodes comprises a ground electrode and an inherently non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a signal electrode and a non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power electrode and a non-contact electrode, respectively.

An electronic assembly comprising: a back electrode electronic part comprising: a main body; a circuit, and electrodes arranged on an outer back surface of the main body, wherein the electrodes comprise integration possible electrodes and general electrodes; a plurality of the integration possible electrodes are arranged adjacently to each other to form a group of integration possible electrodes; said electronic assembly further comprising: a printed circuit board 1 and substrate electrodes arranged on an outer surface of the printed circuit board; wherein: the substrate electrodes comprising a first substrate electrode 34 and second substrate electrodes 2; said integration possible electrodes and said first substrate electrode are connected to a single first solder bump; each of said general electrodes and each of said second substrate electrodes are individually connected to single second solder bumps; and said first solder bump is larger than each of the

second solder bumps; wherein said electrodes of said back electrode electronic part are arranged in a matrix, and said group of integration possible electrodes is arranged at a corner of the matrix; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a signal electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a ground potential electrode; wherein one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a power supply potential electrode; wherein said group of integration possible electrodes is directly connected to said first solder bump; wherein said electrodes arranged on an outer surface of the main body of the back electrode electronic part protrude from said back electrode electronic part so as to support said first and second solder bumps; wherein the outer surface of the main body is a rearmost surface of said back electrode electronic part; wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a ground electrode and a non-contact electrode, respectively; wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a signal electrode and a non-contact electrode, respectively;

wherein a first and second one of said integration possible electrodes of the back electrode electronic part that are part of said group of integration possible electrodes comprises a power electrode and a non-contact electrode, respectively.

A back electrode electronic part comprising: at least one first electrode positioned on an outer rear surface of said electronic part and connected to a first solder bump; at least one second electrode positioned on the outer rear surface of said electronic and connected to a second solder bump wherein said first solder bump has a larger lateral cross section than said second solder bump: and each of said first electrodes and second electrode are arranged in a matrix on said rear surface of said electronic part.

A back electrode electronic part comprising: a main body including a circuit; and electrodes arranged for solder bumps and supported on an outer back surface portion of said electronic part and connected to said circuit; wherein said electrodes are arranged into groups of electrodes at portions of the electrode arrangement at least one of said groups of electrodes 15 is connected to a first solder bump which is larger than second solder bumps connected to said electrodes 4 arranged other than in said groups of electrodes; the electrodes arranged other than in said groups of electrodes are each connected to only one second solder bump.

To further clarify the disclosure of an inherently non-contact electrode, it is noted that the electrode 15 is not in direct physical contact with another electrode 15; therefore, it a non-contact electrode with respect to direct physical contact with another electrode.

However, Dockerty does not appear to explicitly disclose that the first electrodes are spaced apart by the same distance that the second electrode is spaced apart from a nearest one of the first electrodes; wherein each of the electrodes are the same size; wherein a first distance between a first and second one of the plurality of integration electrodes forming the group of integration possible electrodes is the same as a second distance between the first one of the plurality of integration electrodes and a nearest one of the general electrodes; wherein said first substrate electrode of said printed circuit board is larger than each of said second electrodes of said printed circuit board.

Regardless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not disclosed that, in view of the applied prior art, the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using other dimensions. Indeed, it has

been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical.

Also, although Dockerty does not appear to explicitly disclose that each of the integration possible electrodes that are part of the group of integration possible electrodes inherently have a substantially same potential level when said circuit operates, the limitation, "when said circuit operates," is a statement of intended use which does not result in a structural difference between the claimed electrodes and the electrodes of Dockerty. Further, because the electrodes of Dockerty are inherently capable of being used as intended, the statement of intended use does not patentably distinguish the claimed electrodes from the electrodes of Dockerty.

In any case, as cited supra, Barrow discloses that each of the integration possible electrodes 18 that are part of the group of integration possible electrodes inherently have a substantially same potential level when said circuit operates because they are electrically interconnected by bump 26. In addition, it would have been obvious to combine the bump interconnected electrodes of Barrow with the product, including the first solder bump 16/33 of Dockerty, because it would facilitate the disclosure of Dockerty of "a continuum of solder extending from one solder ball to a succeedingly located solder ball," "support elements . . . extend . . . over

multiple solder ball spacing increments. For example, support solder 16 extends over 4 solder spacing increments while support solder 17 extends over three increments. Support solder 18 only extends one solder ball increment in each axial direction while remaining symmetrically within the range of the pattern defined by the support solder 16," and "while the other axis defines a continuum between solder ball locations."

Relatedly, although Dockerty does not appear to explicitly disclose wherein four integration electrodes form the group of integration possible electrodes; wherein three integration electrodes form the group of integration possible electrodes, as cited supra, Barrow discloses wherein three or four "at least two" integration electrodes 18 form the group of integration possible electrodes. Again, it would have been obvious to combine the bump interconnected electrodes of Barrow with the product, including the first solder bump 16/33 of Dockerty, because it would facilitate the disclosure of Dockerty of "a continuum of solder extending from one solder ball to a succeedingly located solder ball," "support elements . . . extend . . . over multiple solder ball spacing increments. For example, support solder 16 extends over 4 solder spacing increments while support solder 17 extends over three increments. Support solder 18 only extends one solder ball increment in each axial direction while remaining symmetrically within the range of the pattern defined by the support solder

16," and "while the other axis defines a continuum between solder ball locations."

Claims 3, 9, 27-29 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dockerty and Barrow as applied to claims 1 and 7 supra, and further in combination with Kaneshiro (JP10-56093).

Dockerty and Barrow do not appear to explicitly disclose wherein one of the integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode which is not connected to said circuit, and wherein a second one of said integration possible electrodes that are part of said group of integration possible electrodes comprises a non-contact electrode.

Nevertheless, in the figures, and English translation and abstract, Kaneshiro discloses one of integration possible electrodes 10 of a group is a non-contact electrode (associated with "non contact electrode (N)") which is not connected to a circuit. Moreover, it would have been obvious to provide the electrode of Dockerty and Barrow with the non-contact property of Kaneshiro because, as taught by Kaneshiro, it would improve connection strength and reliability and facilitate production of a BGA device ("double with the specification of a BGA type semiconductor device").

Applicant's amendment and remarks filed 5-20-4 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant contends that Barrow does not disclose that the first solder bump is larger than each of the second solder bumps because, "*Barrow* does not disclose that the radially outer contact pads 18 can be split into two separate pads and joined by a single solder joint 26."

This contention is respectfully deemed unpersuasive and is traversed because Barrow is not relied on for a disclosure that the radially outer contact pads 18 can be split into two separate pads and joined by a single solder joint 26. In any case, the disclosure of Barrow at column 2, lines 42-45, "As shown in FIG. 5, some of the contact pads 18 can be formed in proximity with each other so that two adjacent solder balls reflow into a single solder joint 26," and the claim 1 limitation, "a single solder joint that is attached to at least two adjacent contact pads," encompasses the "radially outer contact pads 18."

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
3-Aug-04